

FIG. 1
PRIOR ART

FIG. 2
PRIOR ART

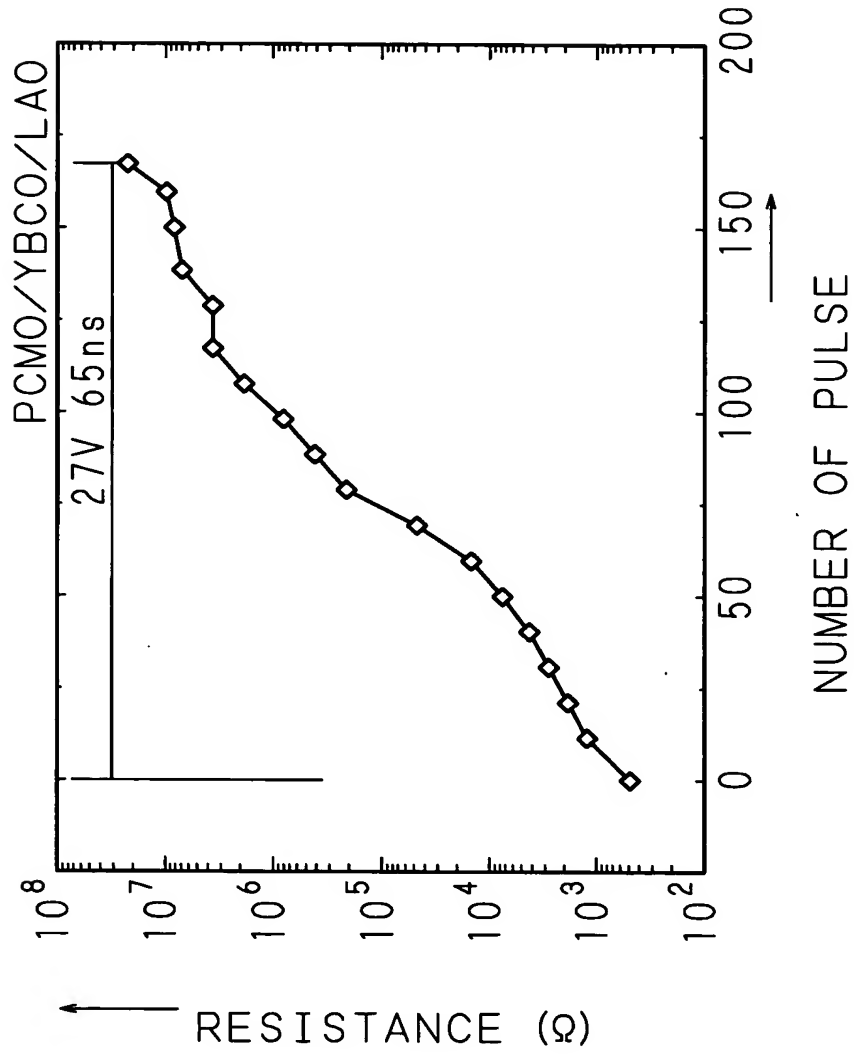


FIG. 3
PRIOR ART

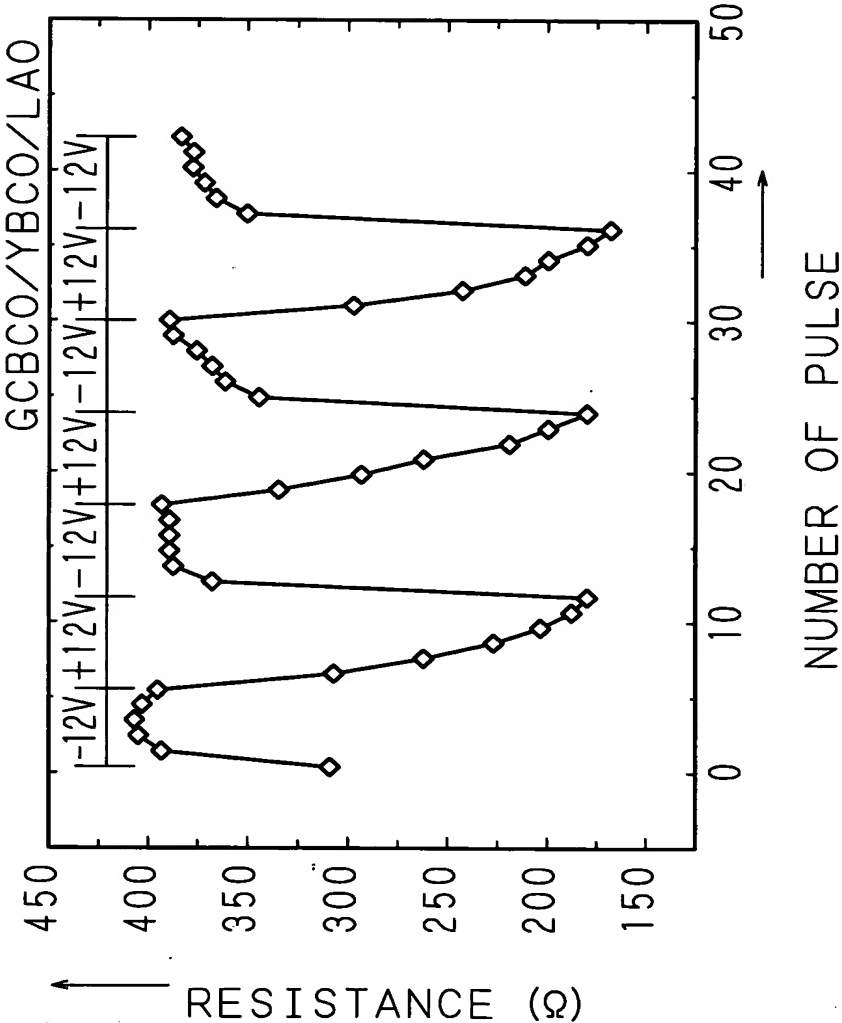


FIG. 4
 PRIOR ART

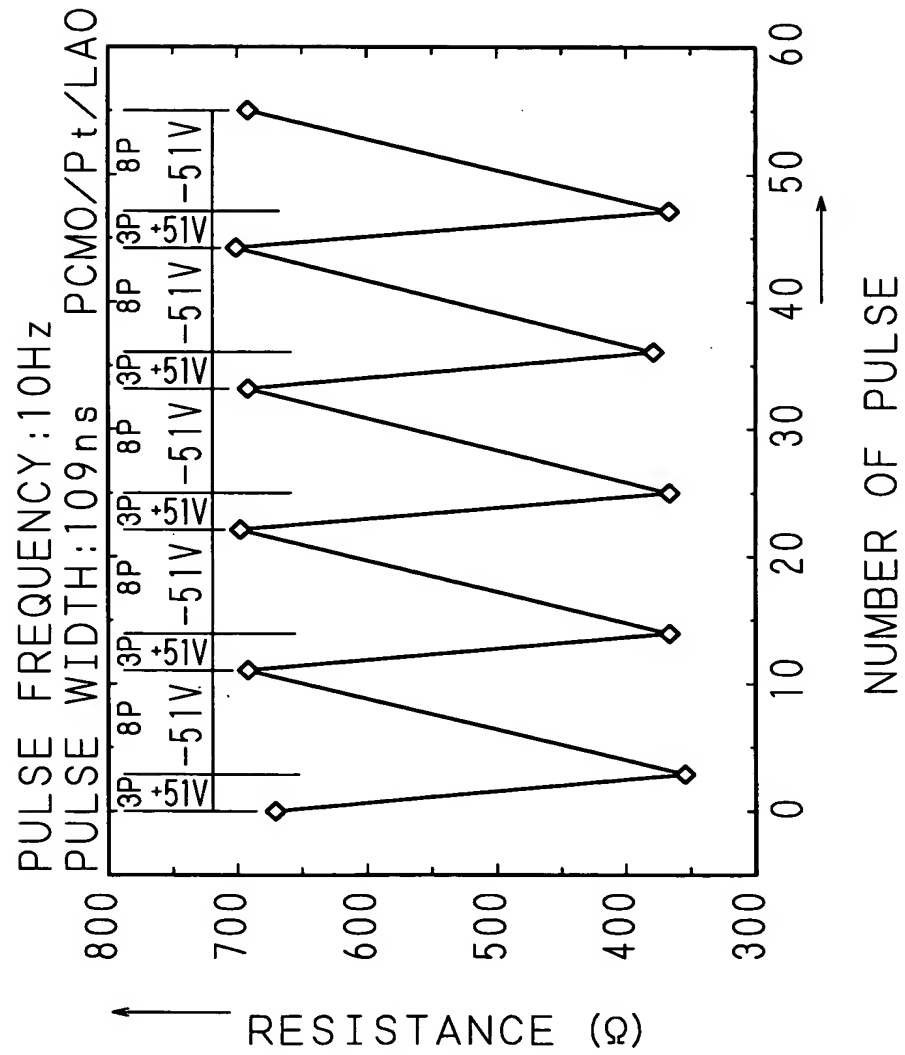


FIG. 5A

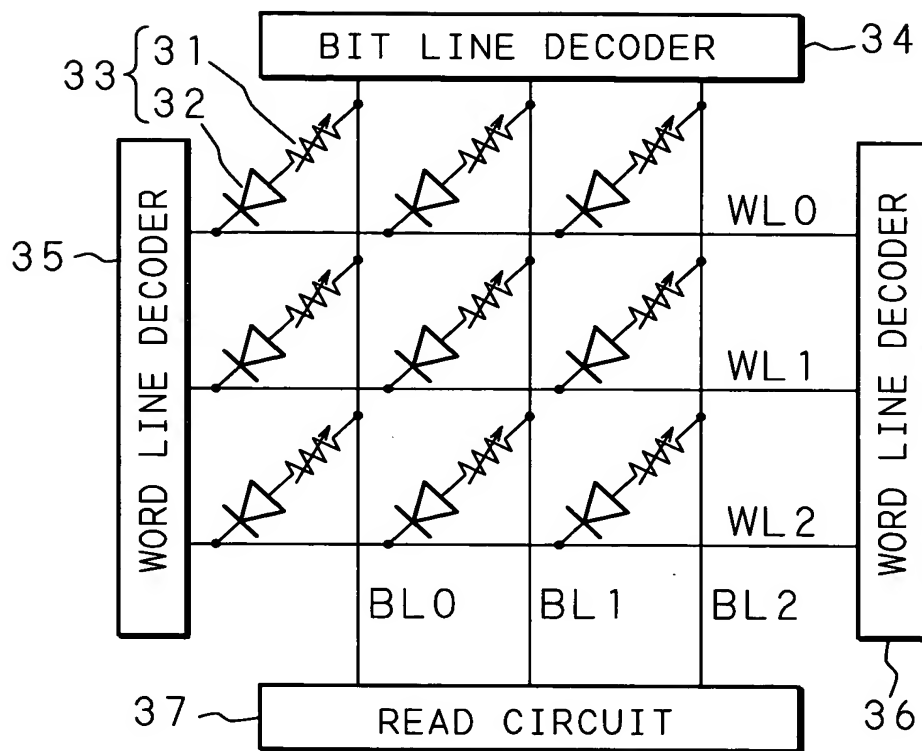


FIG. 5B

	VOLTAGE (BL)	VOLTAGE (WL)
SELECTED CELL	V_w	0
HALF-SELECTED CELL (BL SELECTION)	V_w	$V_w/2$
HALF-SELECTED CELL (WL SELECTION)	$V_w/2$	0
NON-SELECTED CELL	$V_w/2$	$V_w/2$

FIG. 6

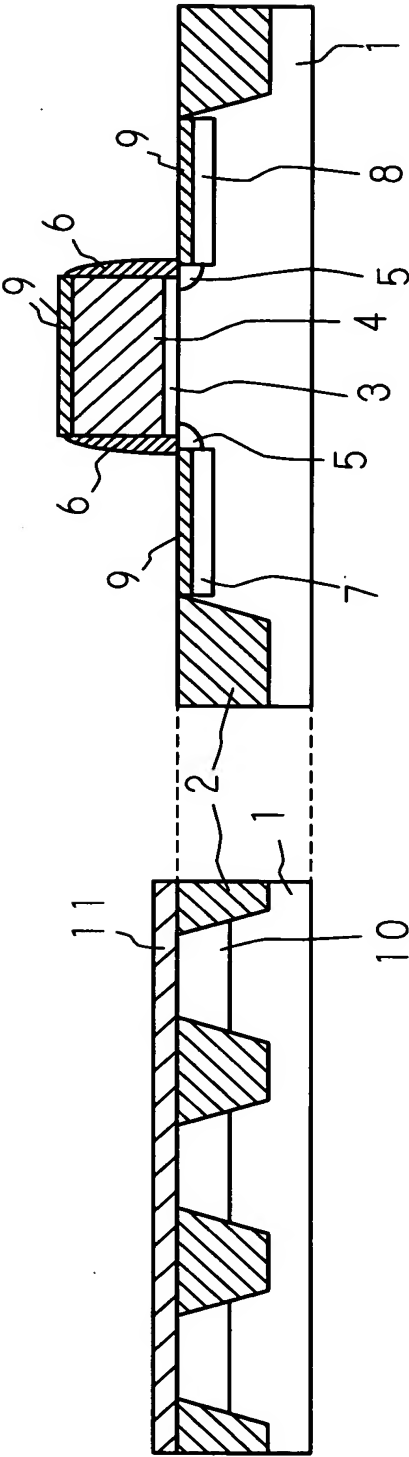
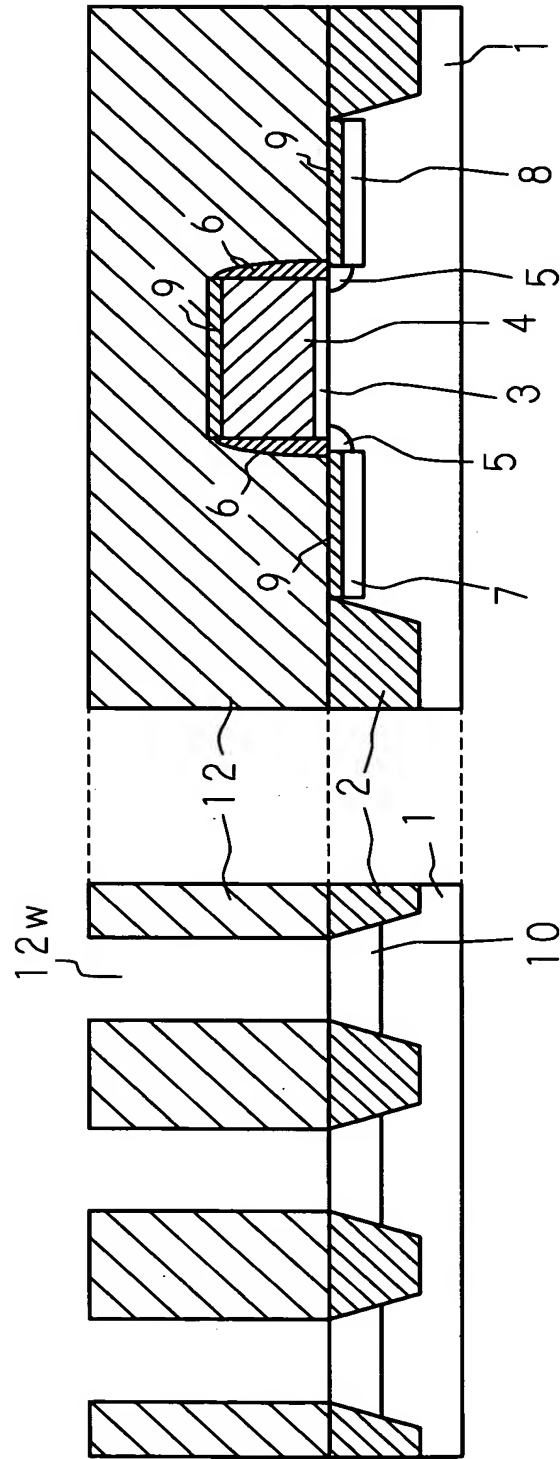


FIG. 7



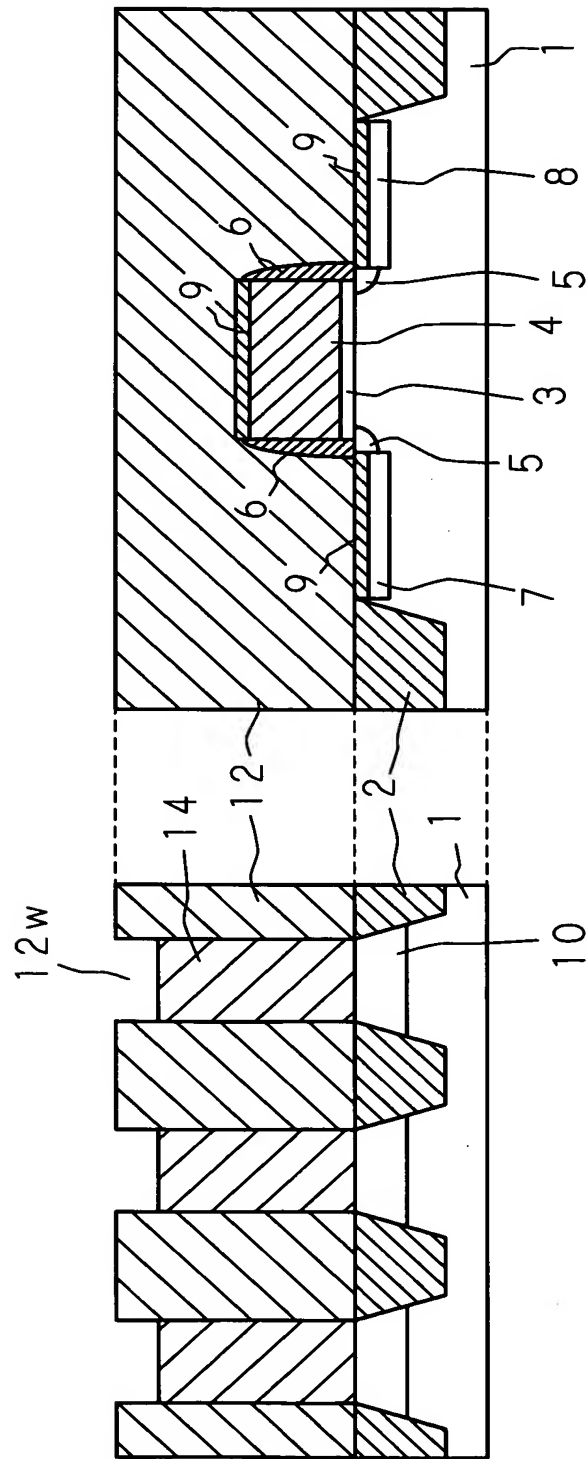
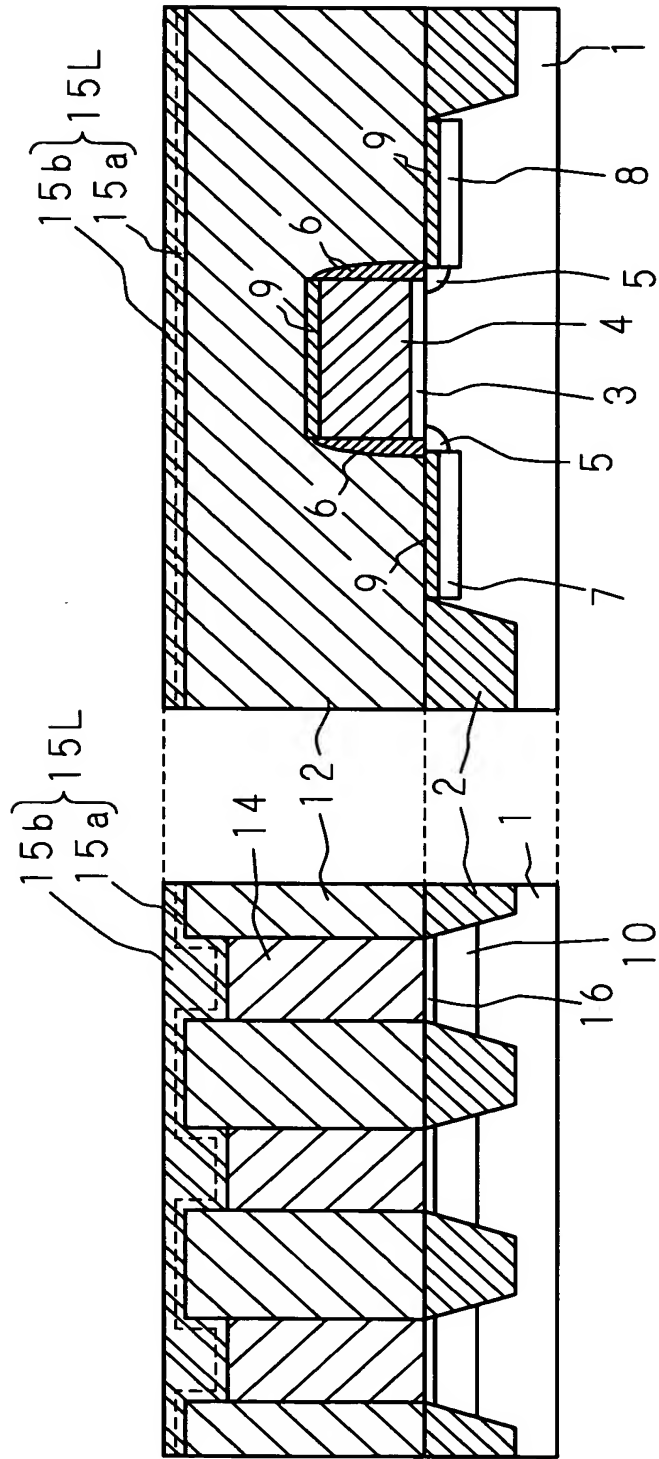
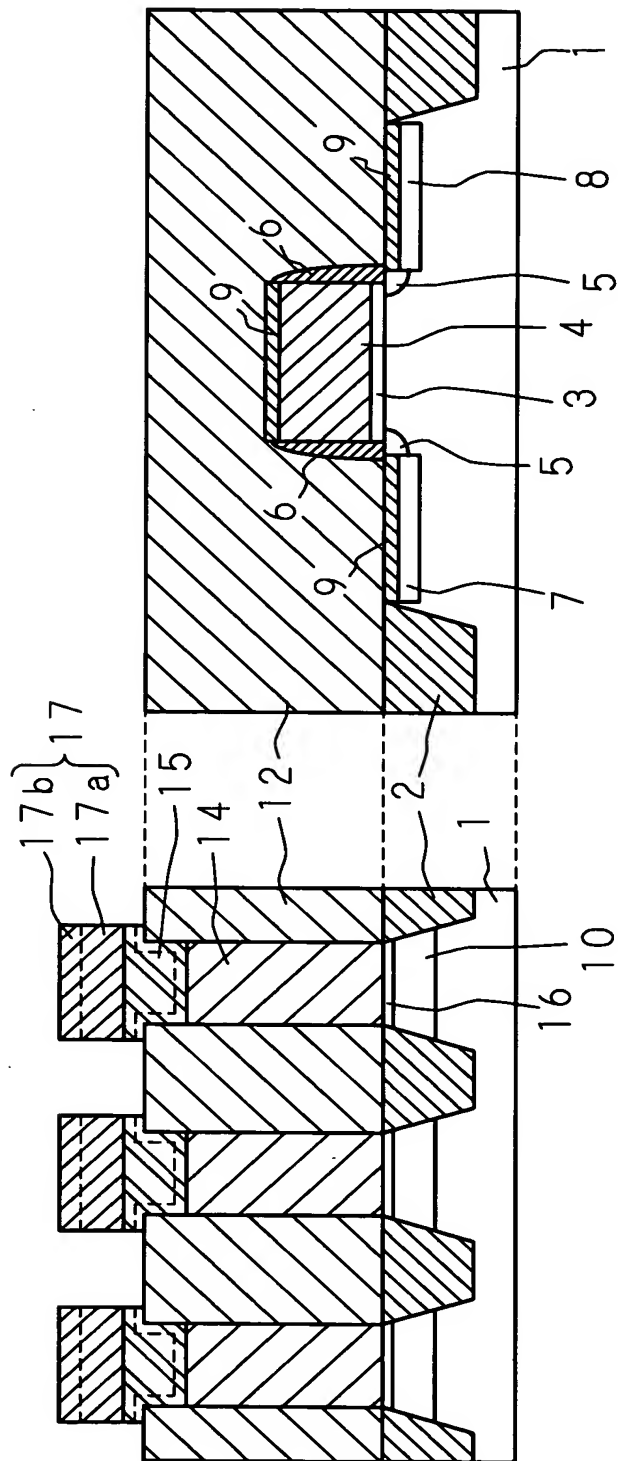


FIG. 8

FIG. 9





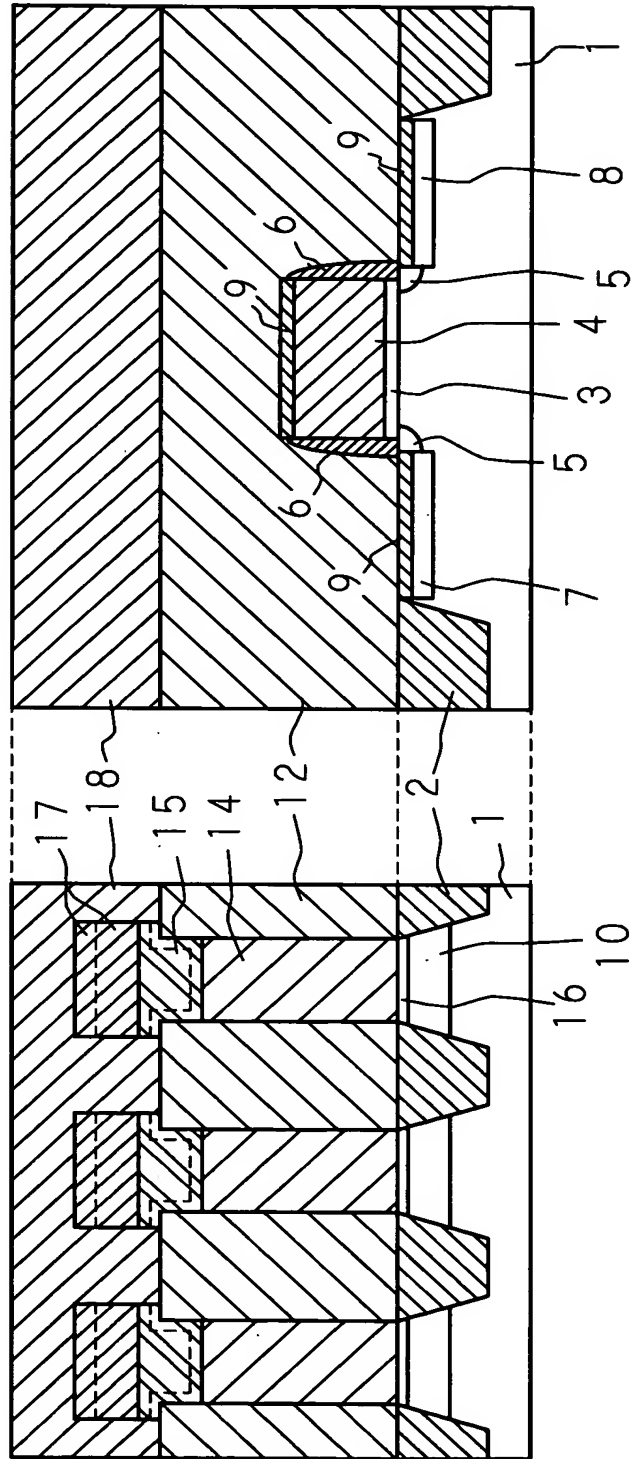


FIG. 11

FIG. 12

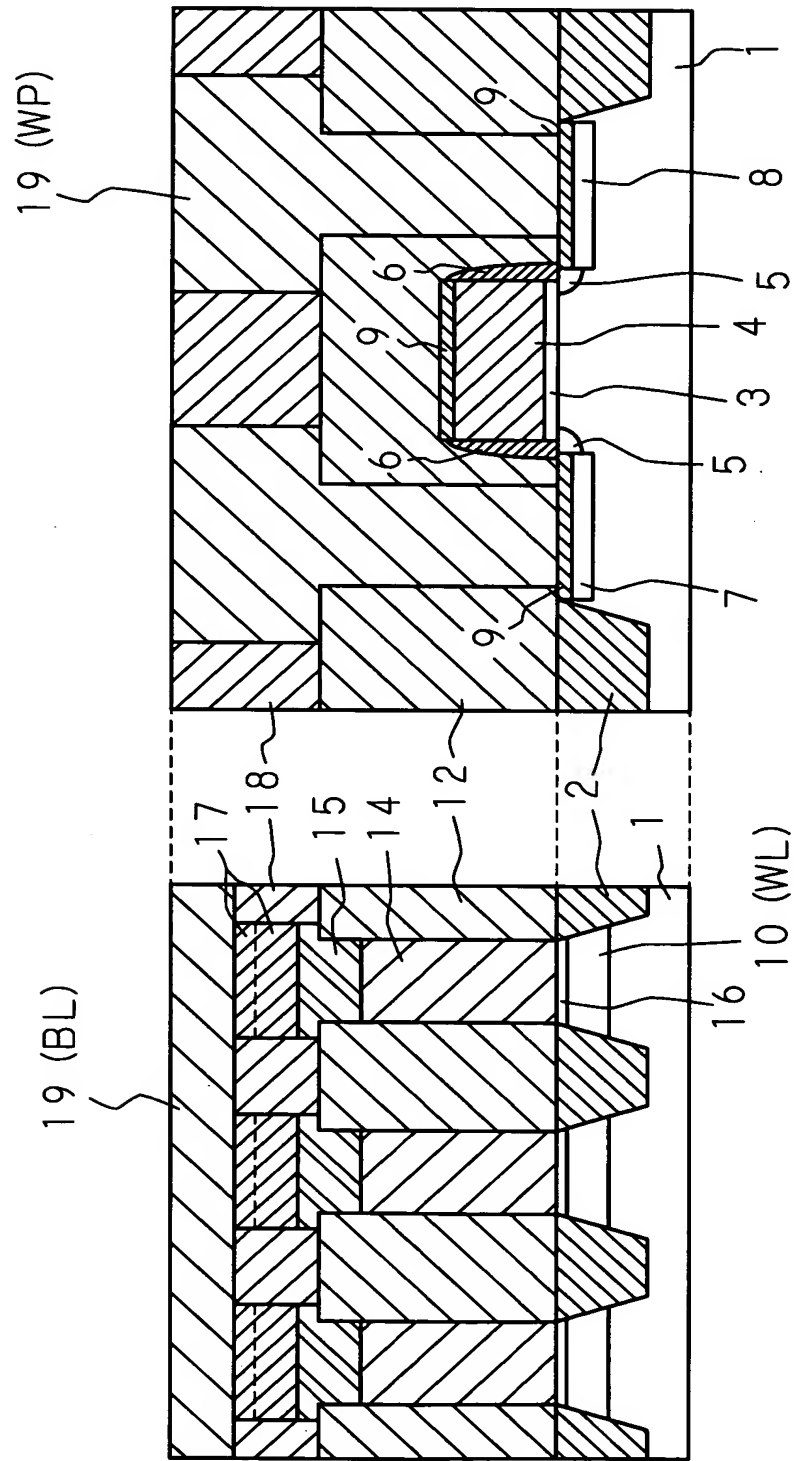


FIG. 13

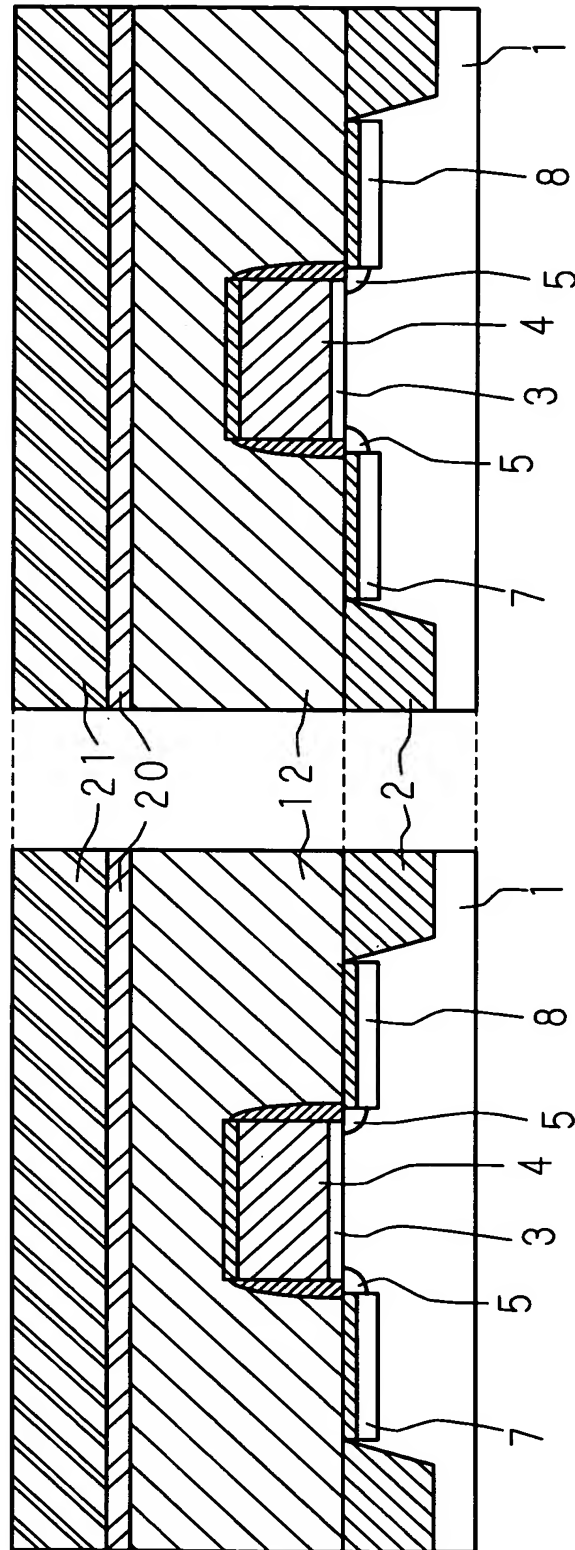


FIG. 14

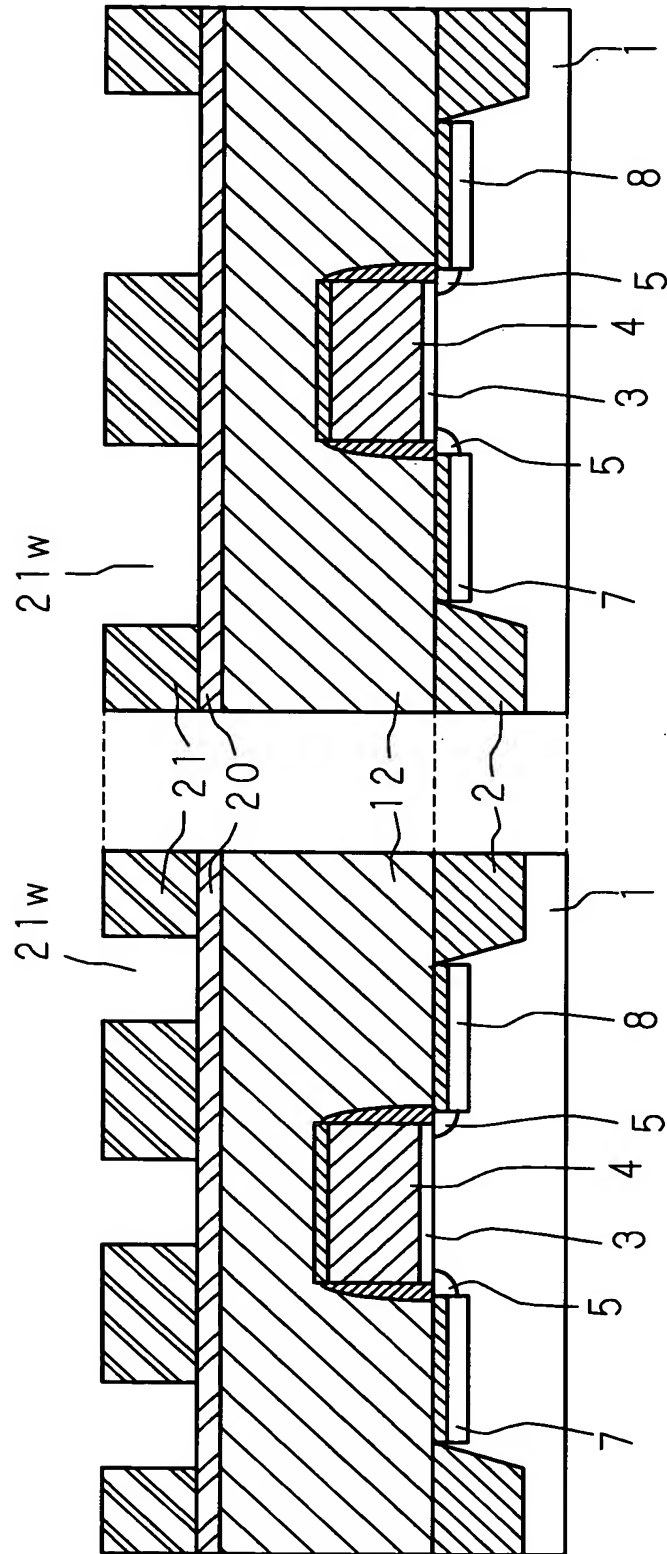
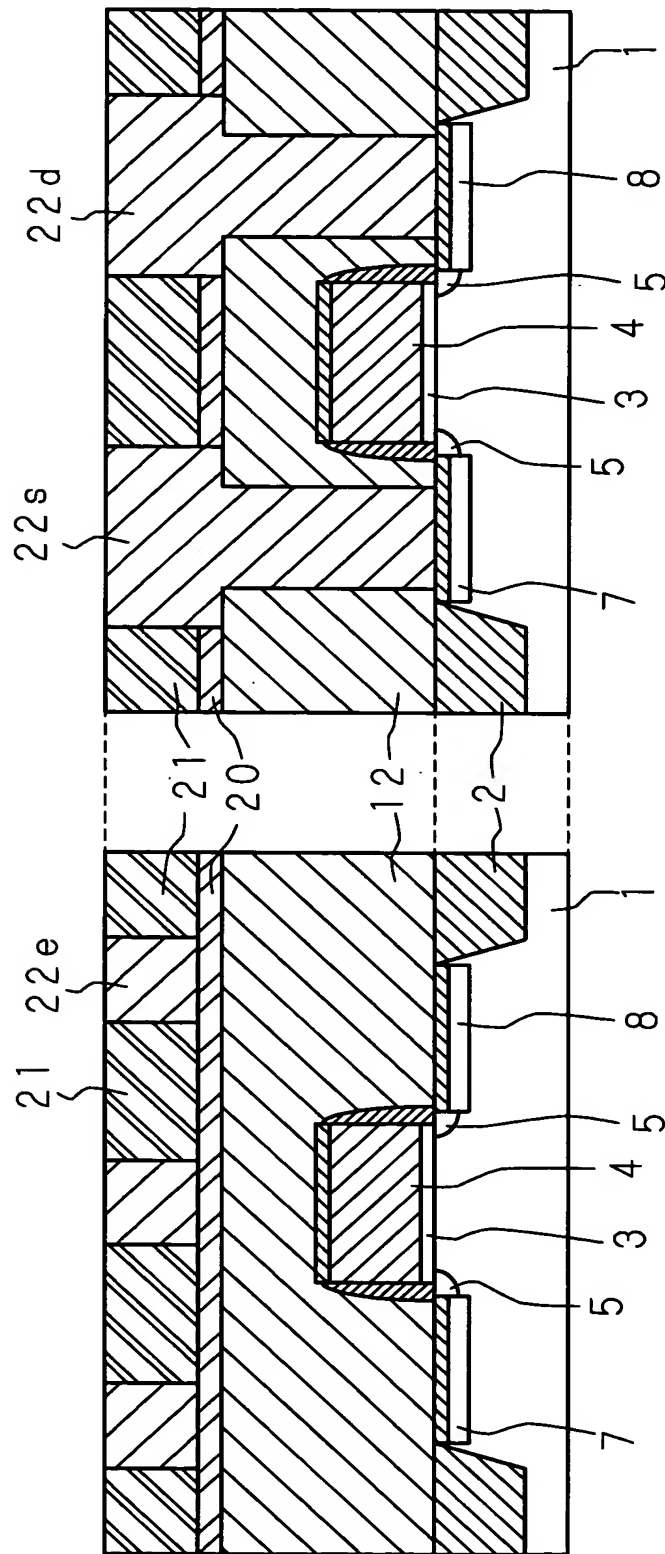


FIG. 15



The figure shows two cross-sectional views of semiconductor devices, labeled 22e (left) and 22s (right). Both devices have a common substrate 1. A gate stack 8 is formed on the surface of the substrate. The gate stack includes a gate dielectric layer 5 and a gate electrode layer 7. In device 22e, the gate electrode layer 7 is patterned to form a gate electrode 3. In device 22s, the gate electrode layer 7 is patterned to form a gate electrode 3 and a side contact 5. The side contact 5 is positioned between the gate electrode 3 and the source/drain regions 2. The source/drain regions 2 are formed by implanting dopants into the substrate 1. The top surface of the source/drain regions 2 is covered by a passivation layer 20. The passivation layer 20 has openings 21 and 23L. The openings 21 and 23L are filled with a conductive material 24a and 24b, respectively. The conductive material 24a and 24b are part of a larger conductive layer 24L.

FIG. 17

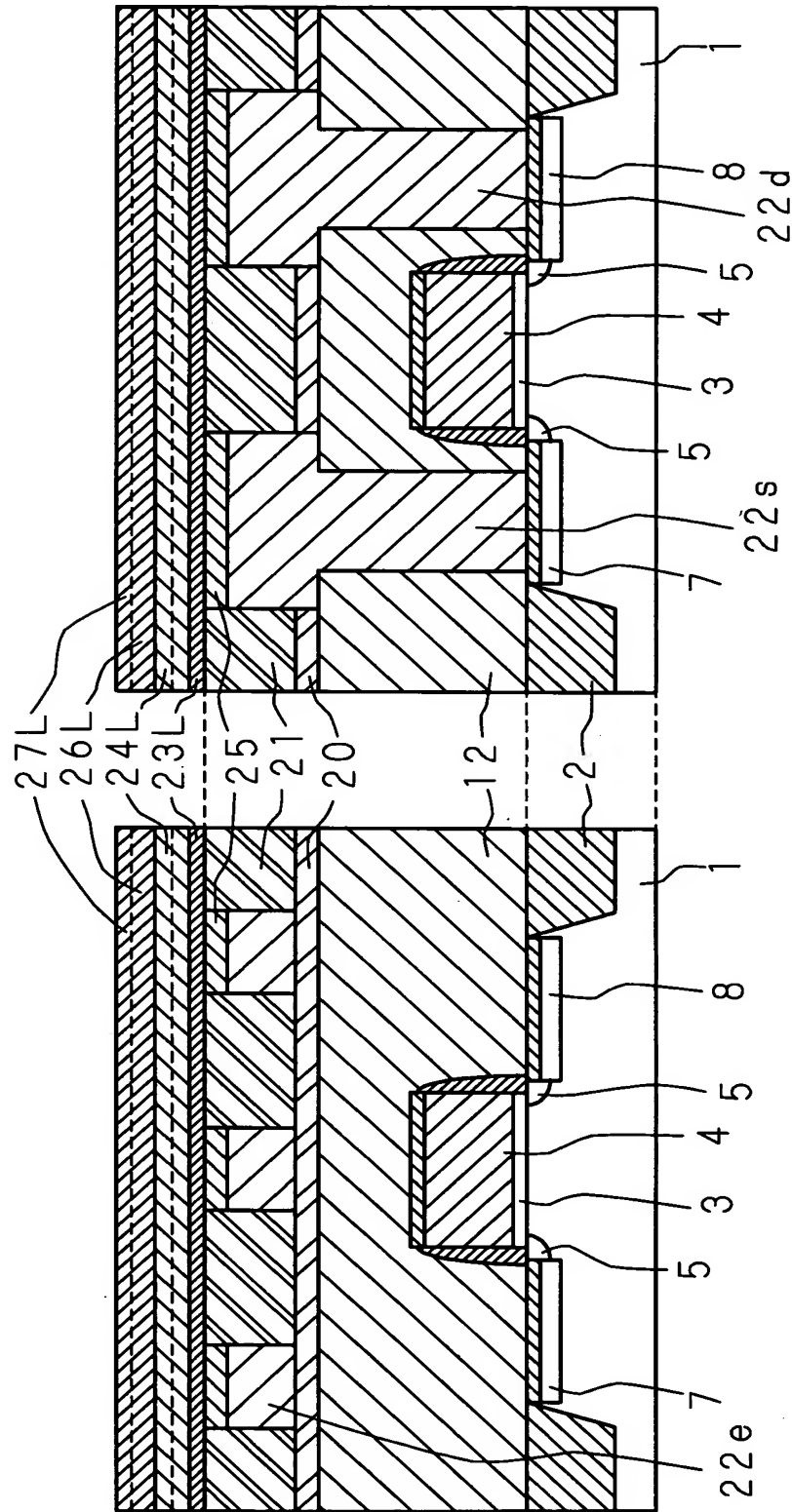


FIG. 18

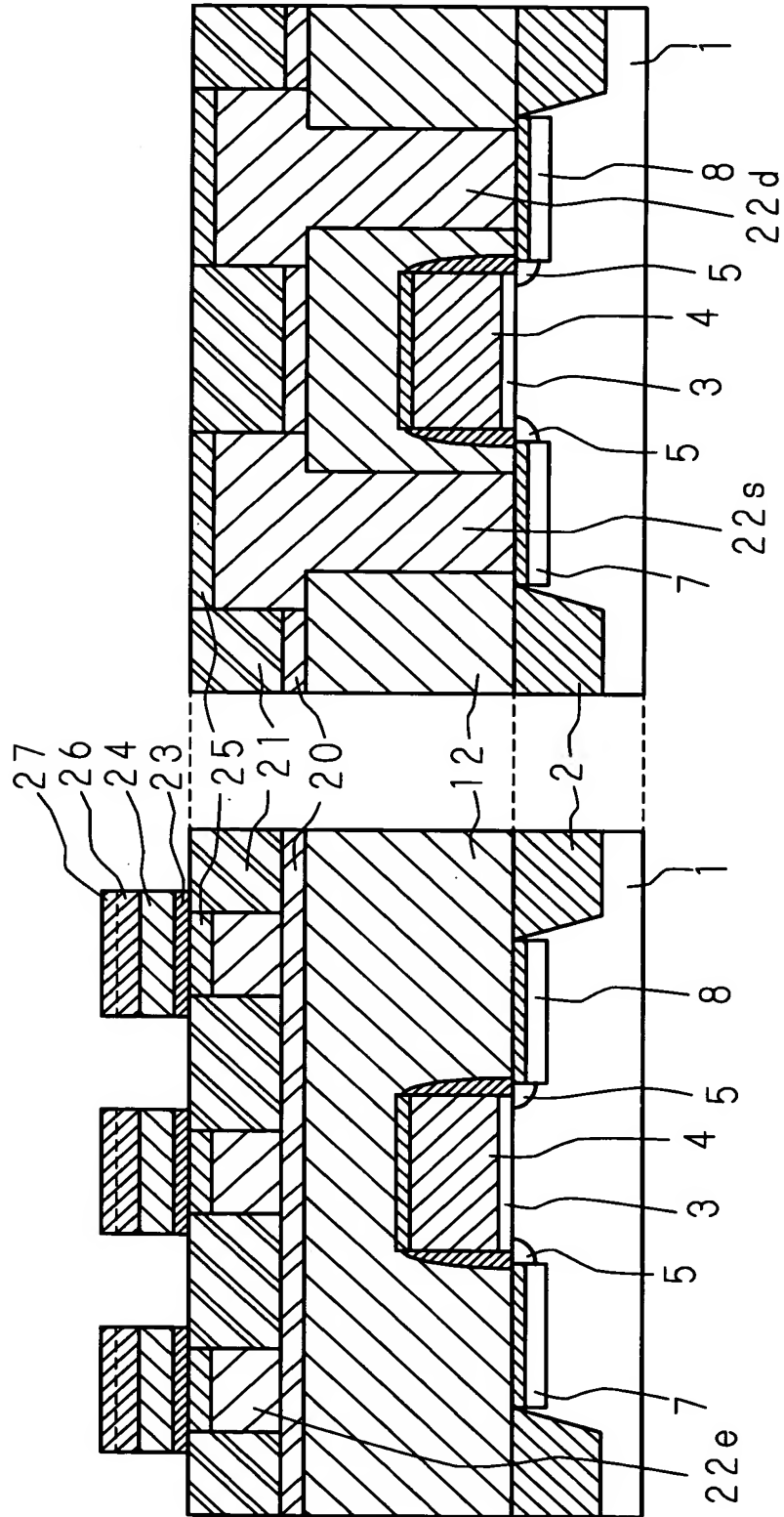


FIG. 19

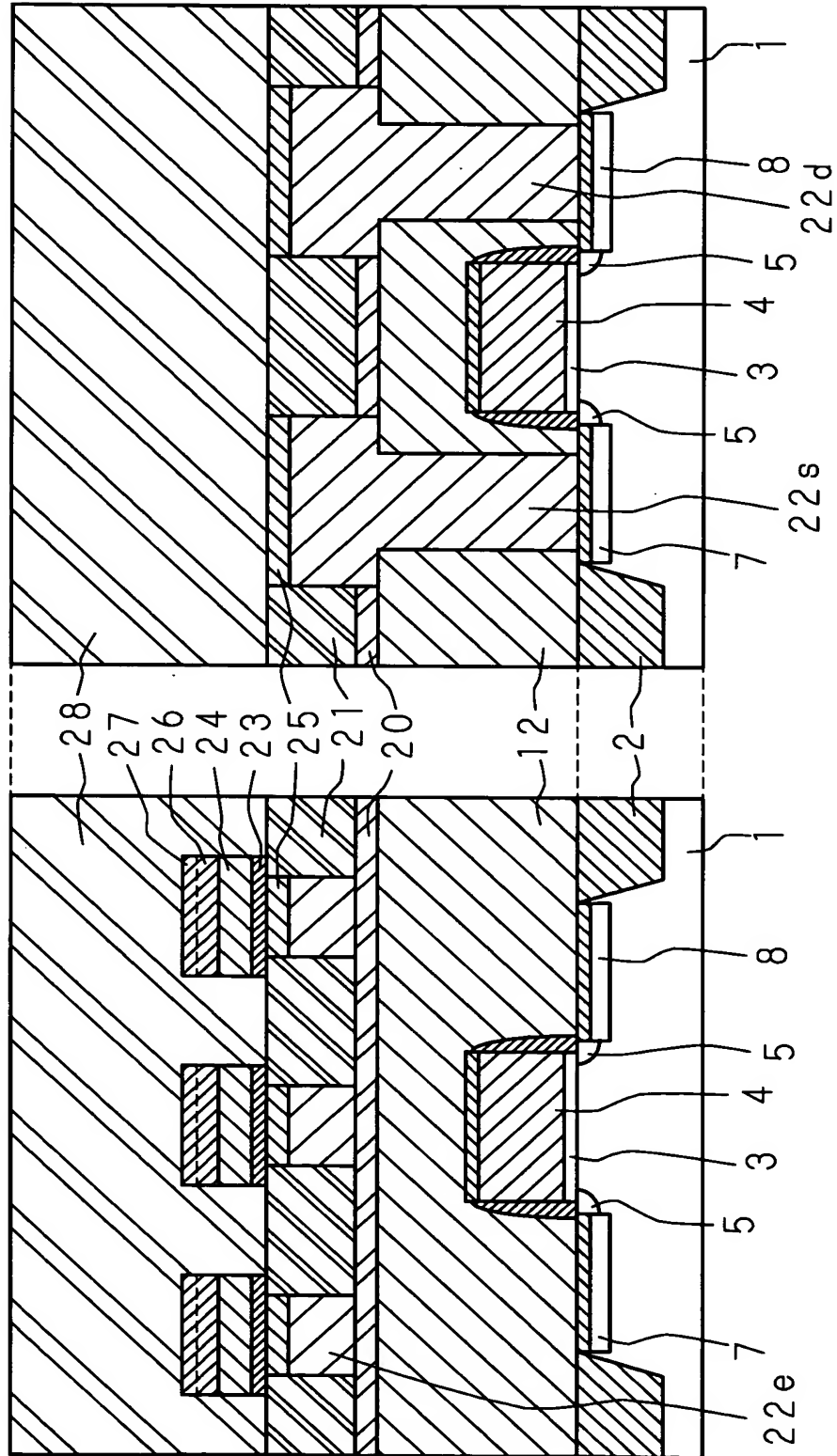


FIG. 20

